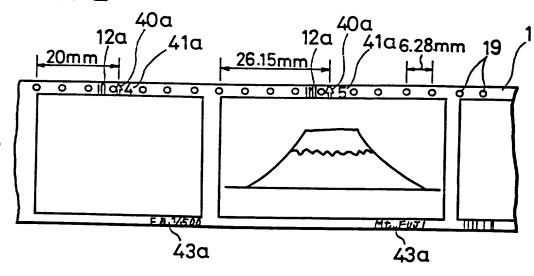


F/G./

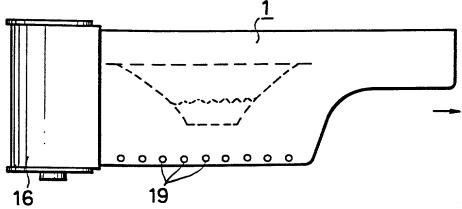
FIG.2



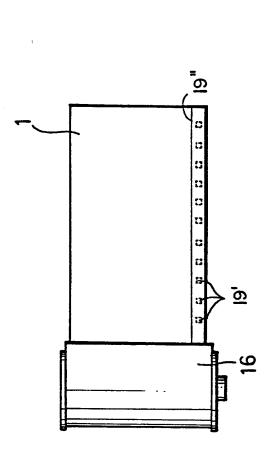
F/G.3A

16

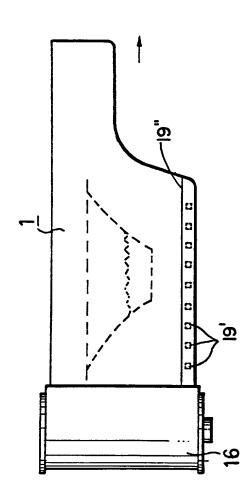
FIG.3B



F16.44



F16.4B



F/G. 5

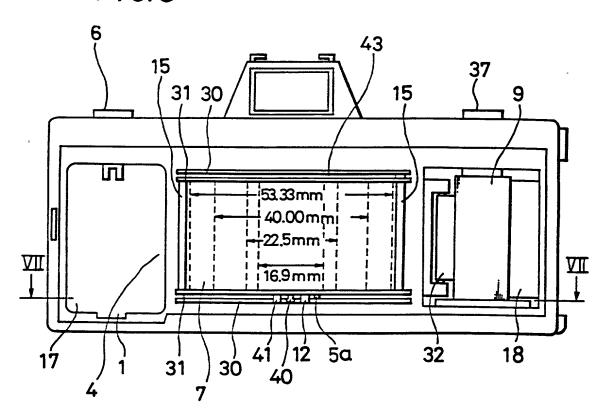


FIG.6

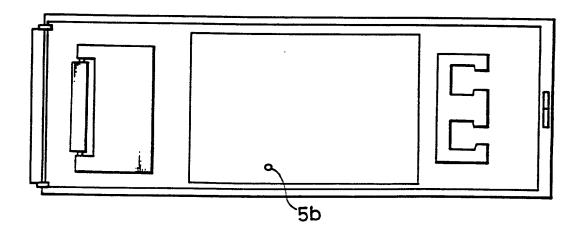
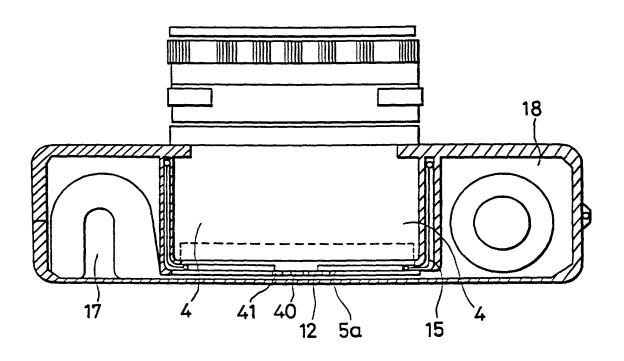
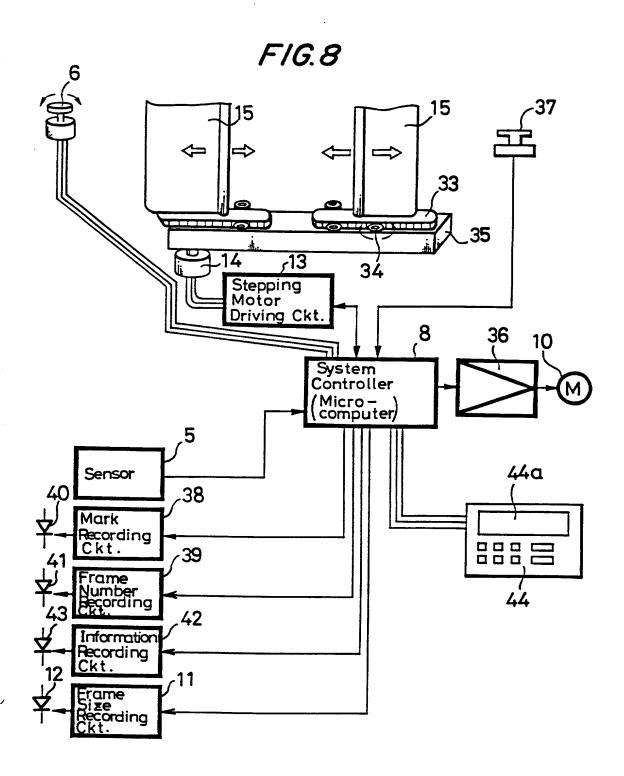


FIG.7





F1G.9

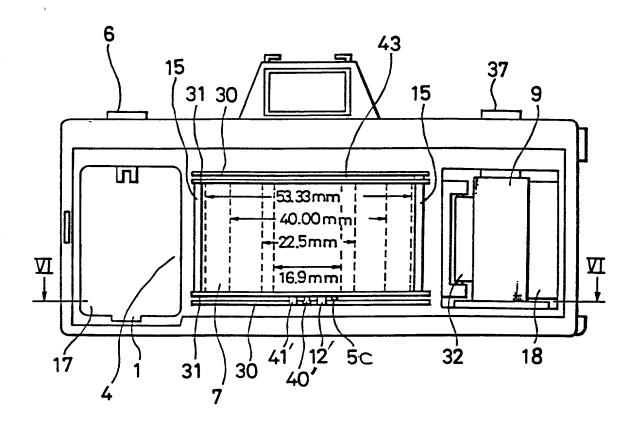
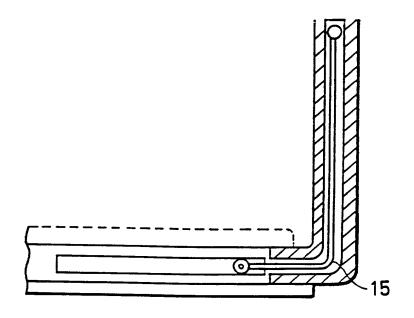
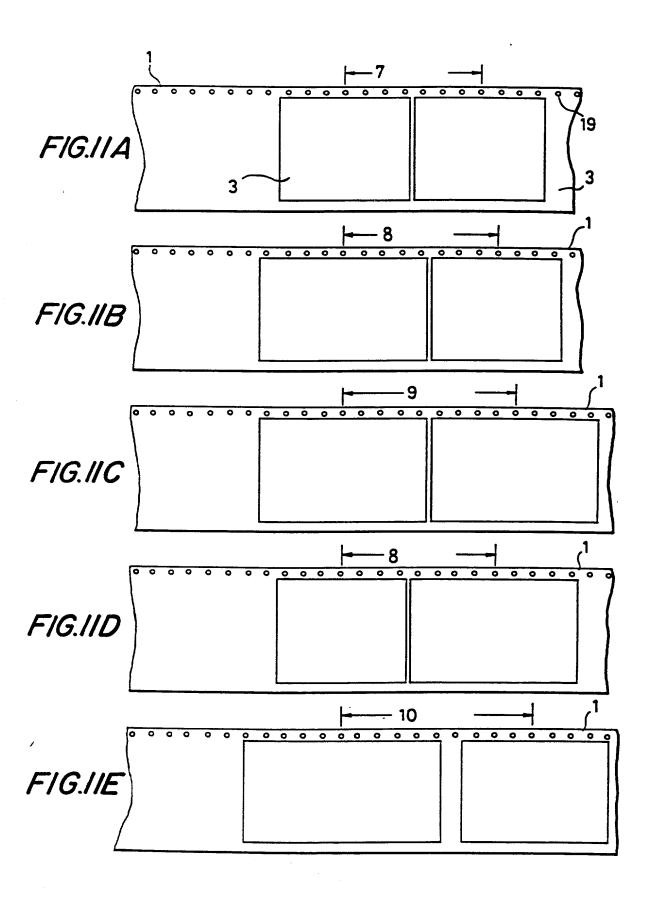


FIG.10





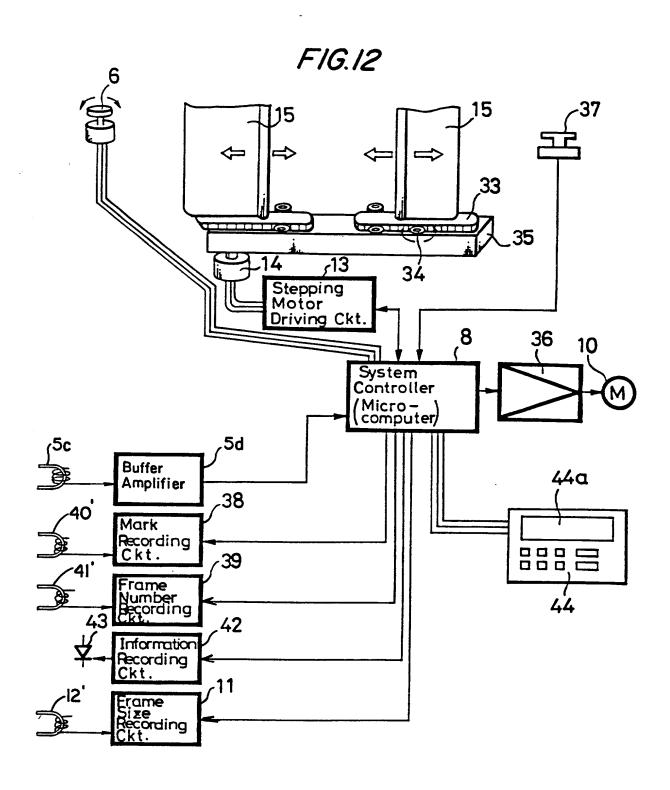
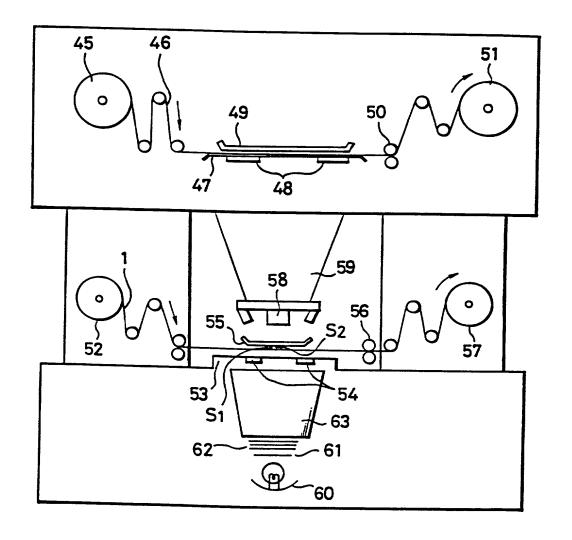


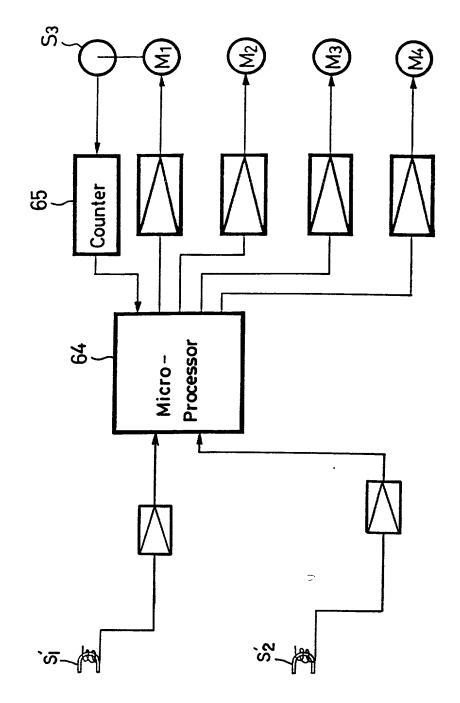
FIG. 13

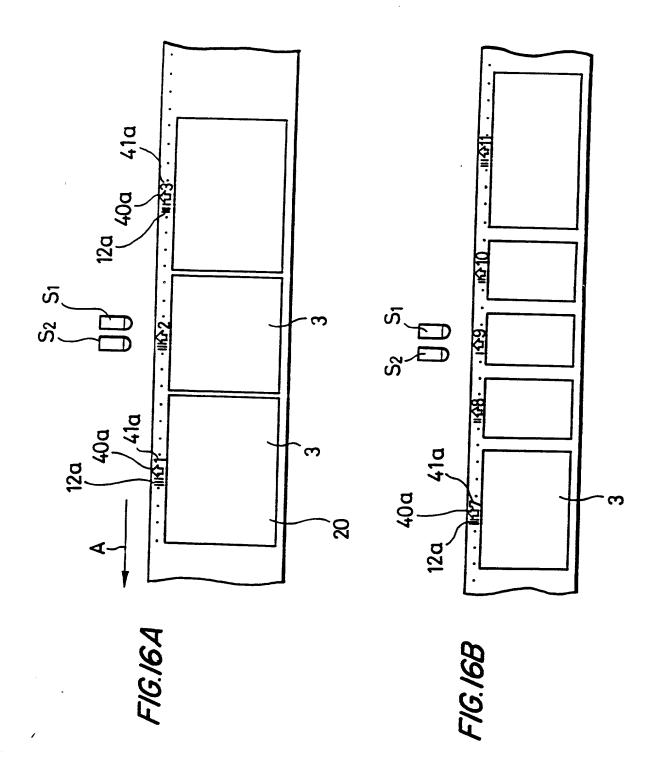


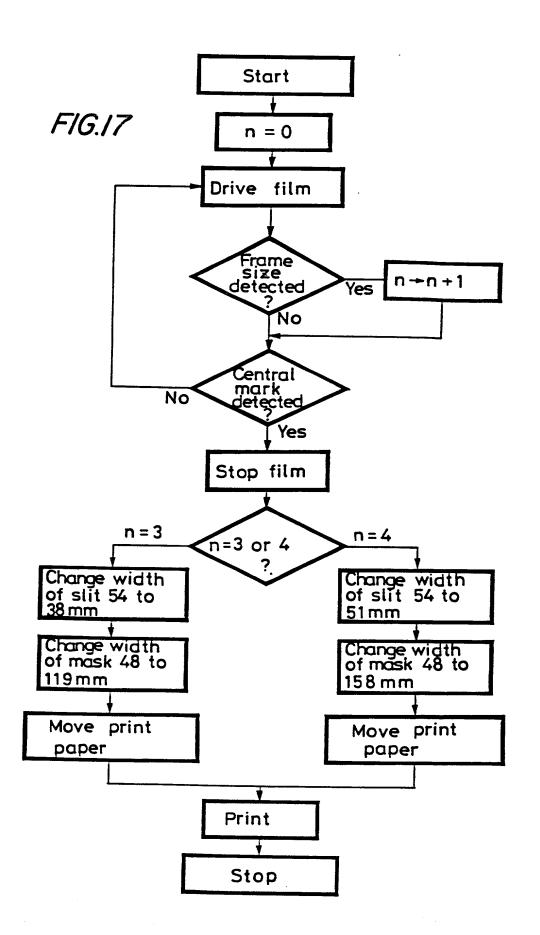
Counter 65 Micro – Processor S₁ Vcc + → cc → **2**′

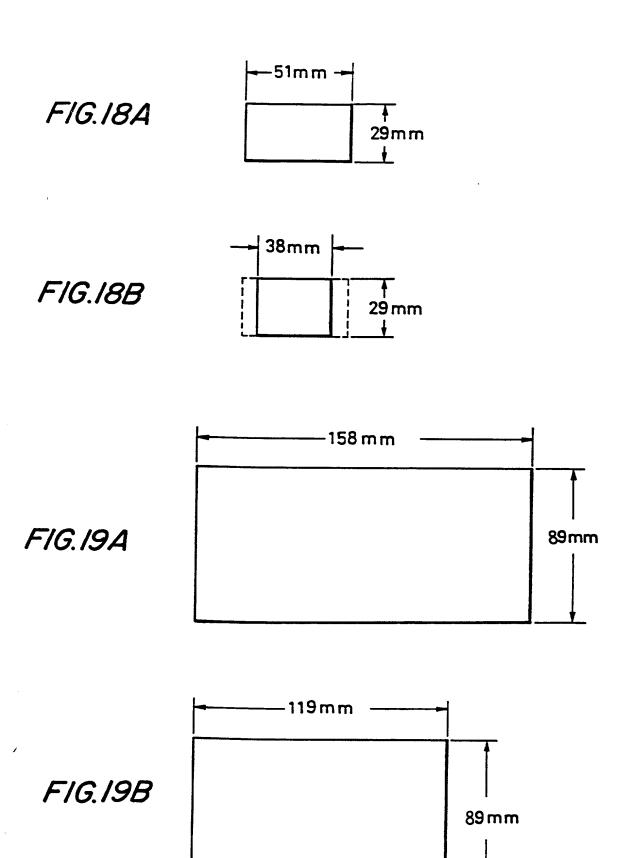
F1G.14

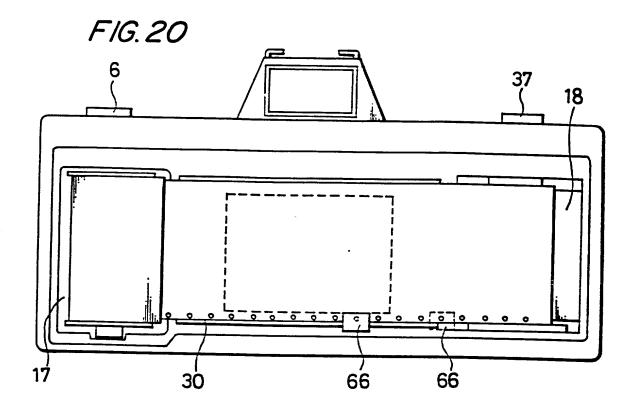
F1G.15

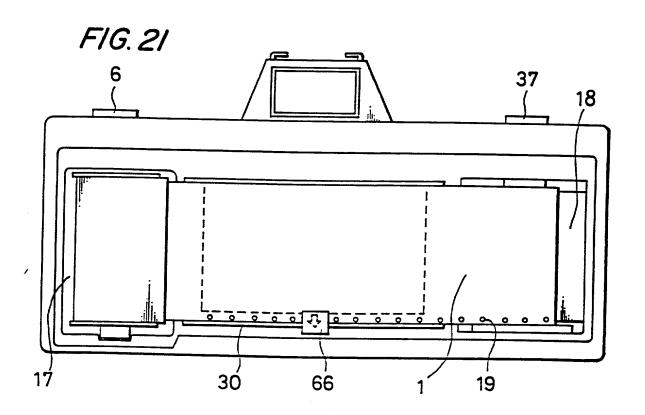












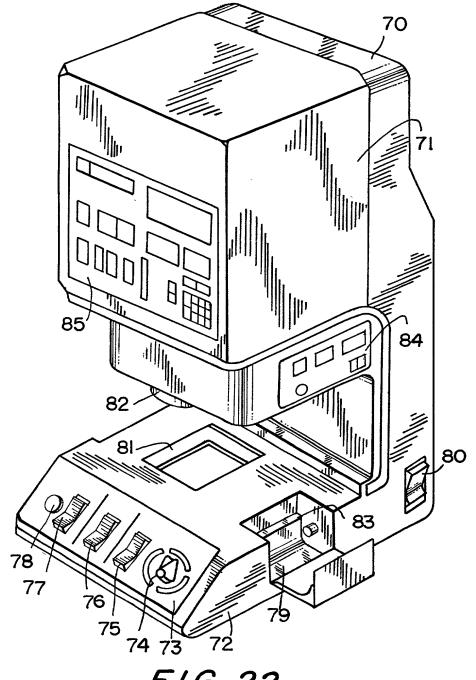
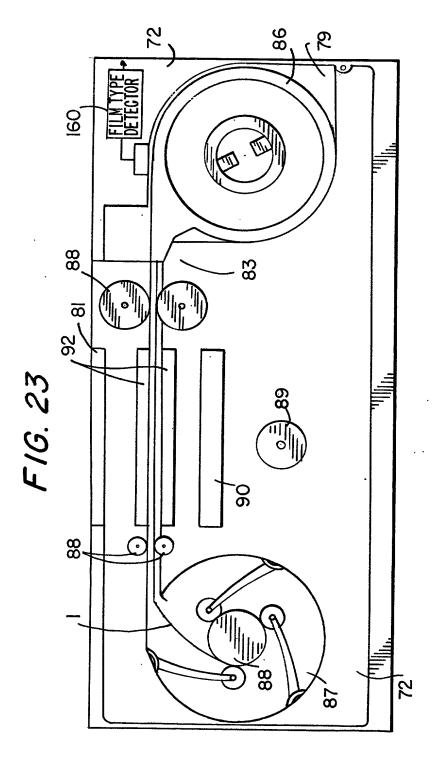
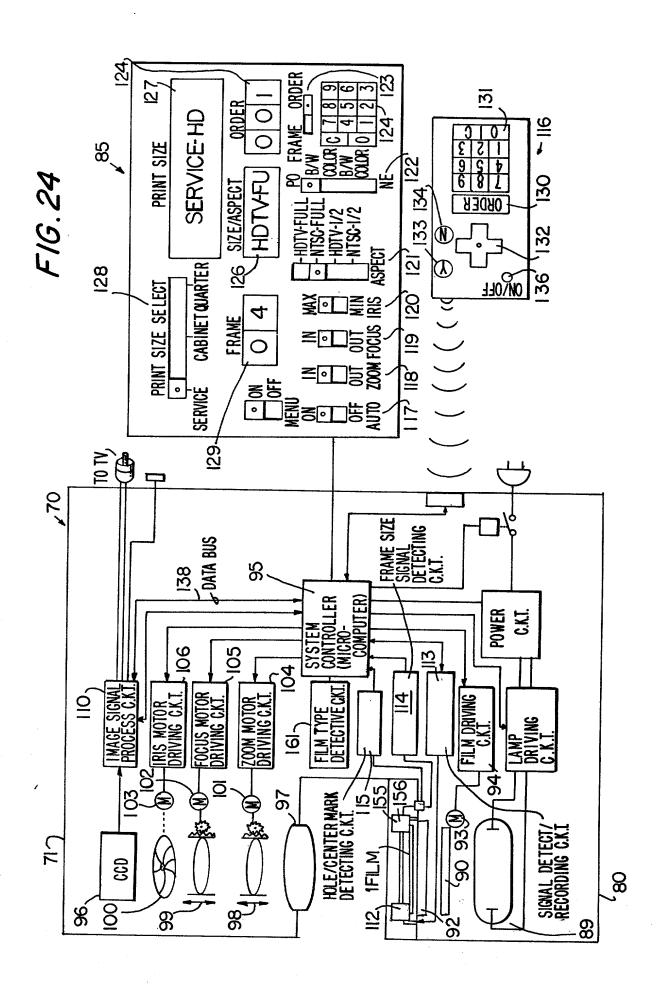
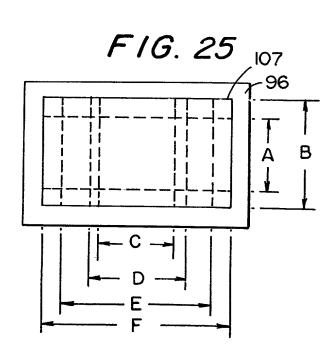
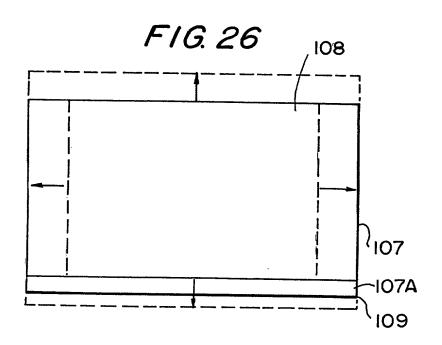


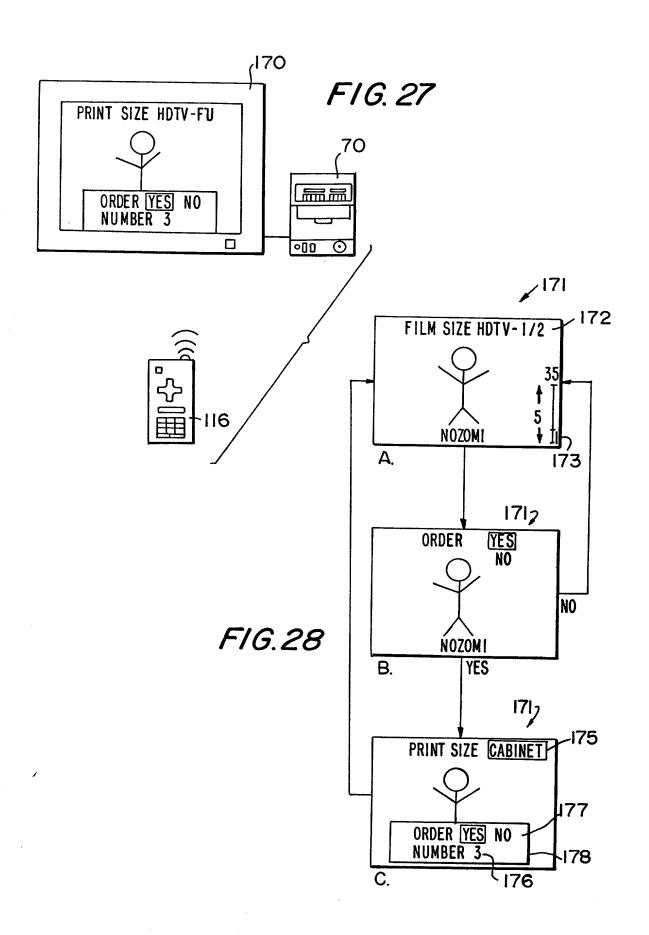
FIG. 22

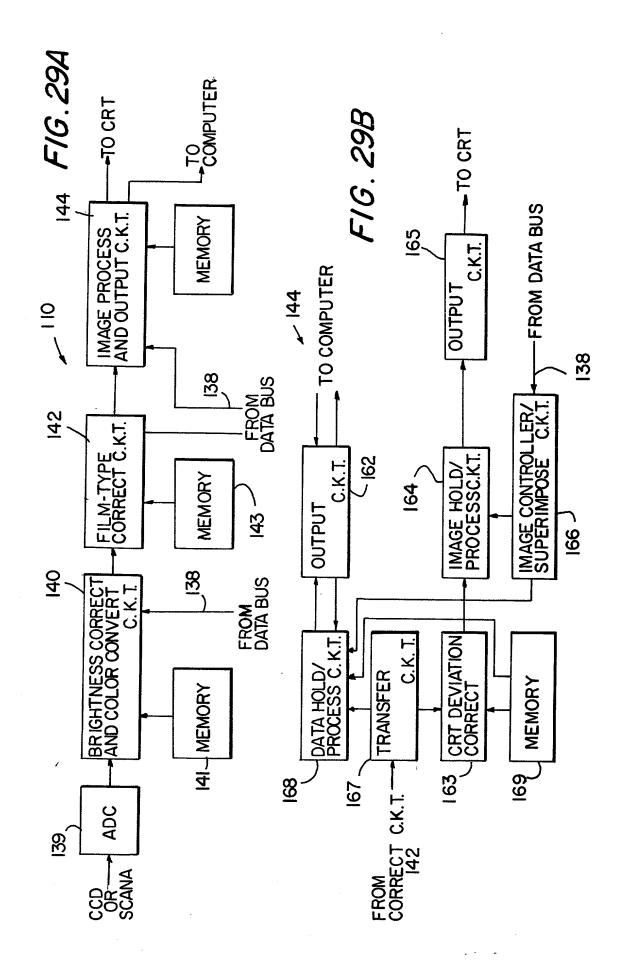


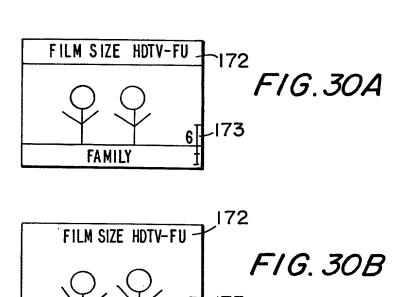


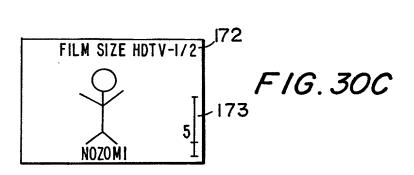


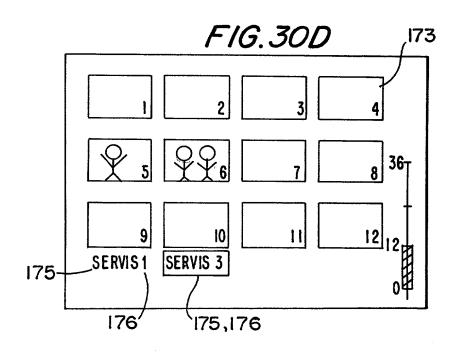


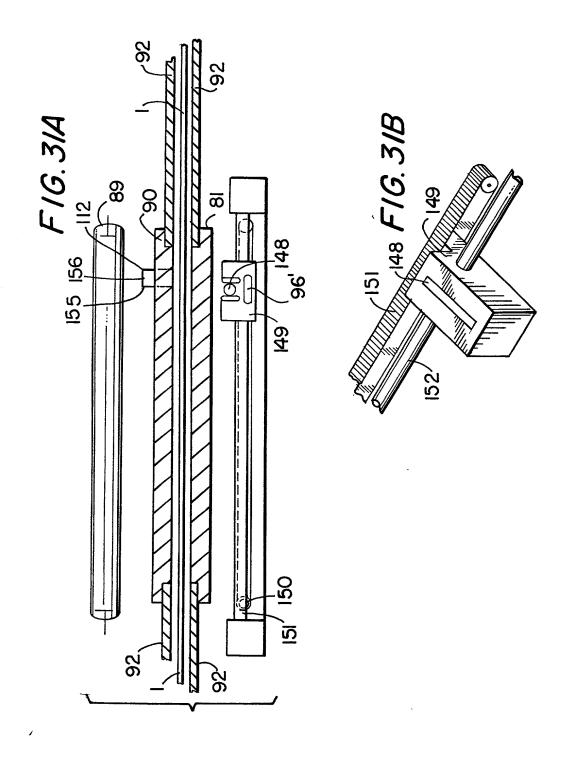


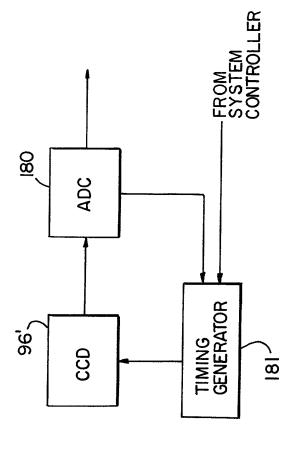












F16.32